

**PATENT**  
**IBM Docket No. RAL9-99-0157**

**REMARKS**

This amendment filed with a Request for Continued Examination is in response to the Final Office Action mailed February 6, 2004 and presents claims 1-17 for further examination.

The outstanding final rejection rejects claims 1-17 under 35 USC 102(b) as being anticipated by Hedlund (U.S. Patent No. 5,136,584). A rejection under 35 USC 102(b) requires that all the elements recited in the claim including their interconnection is disclosed in a single reference. With reference to claim 1 and the dependent claim the way in which the components are interconnected are specifically recited in the claim. No such connections are shown in Hedlund et al. In particular, the counter and its interconnection to other components in the claim are not shown in the prior art reference. In addition, the second input data bus as recited in the claim or the finite state machine its interconnection and function are not present in the cited reference. Also the limitation that data packets are used directly from the storage and not buffered in a register connected between the storage and said multiplexor is not shown in the reference. In Hedlund register 404 is placed between the storage and MUX 48. As a consequence claim 1 and the dependent claims are patentable over the art of record.

It is noted that the Hedlund reference in Figure 5 does describe a data segmenter, however the data segmenter in Fig. 5 is completely different from the data segmenter claimed in applicants' claims. A cursory look at Figure 5 showing the prior art data segmenter and the claimed segmenter as shown in Figure 2 of applicants' application clearly shows the distinction in which applicants' segmenter is less complex than that of the prior art.

In addition, and with respect to claim 1 the recitation regarding the second input data bus clearly defines over the cited reference. In the cited reference data from the memory is fed into data register 404 from which the fixed packet is formed. With respect to claim 1 the second input data bus specifically states that information read out on it is

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used without storing in a buffer to form the fixed packet. This teaching clearly is inapposite to what is shown in the prior art. As a consequence the reference does not anticipate the claims.

In passing, applicants would like to point out some of the errors made by the Examiner. For example, the Examiner states that claim 7 is described in the reference in columns 5-10. Applicants respectfully disagree with the Examiner since the teaching in claim 7 which is specific to applicants' design is not disclosed in the reference including columns 5-10. If the Examiner still maintains that this claim is taught in the reference, it is requested that he identify with more specificity the elements or portion of the reference that would teach the specific configuration set forth in claim 7.

In addition, the Examiner states claim 8 discloses a similar limitation as claims 1-7 therefore claims 8-17 are rejected by the same reason above. Applicants direct the Examiner's attention to claims 15 and 16 which discloses elements different from what was recited in claims 1-8. The elements recited in claims 15 and 16 are not disclosed in the reference. Therefore, even before the amendments to claims 15 and 16 they would be patentable over the art of record.

It is believed the present amendment answers all the issues raised by the Examiner. Re-examination is hereby requested, and an early allowance of all the claims is solicited.

Respectfully Submitted,

  
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